What is claimed is:

1. A machine-implemented method comprising:

receiving data to be stored in a non-volatile memory device comprising storage cells and a charge pump having a predefined electrical current provisioning capability;

varying a programming number of the storage cells based upon the predefined electrical current provisioning capability of the charge pump; and

pulsing the varying programming number of the storage cells in the memory device to store the received data in the memory device.

2. The method of claim 1, wherein the non-volatile memory device comprises an electrically erasable and programmable non-volatile memory device.

3. The method of claim 2, wherein the storage cells comprise multi-level electrically erasable and programmable non-volatile memory cells.

4. The method of claim 3, wherein said varying the programming number comprises varying the programming number of the storage cells based upon a cell level to be programmed by a pulse.

5. The method of claim 4, wherein said pulsing the varying programming number of the storage cells comprises:

pulsing a first set of cells to push those cells to an intermediate level, the pulsing of the first set of cells occurring in groups of two or more cells, each group having a first size corresponding to the predefined electrical current provisioning capability of the charge pump; and

pulsing a second set of cells to push those cells to a highest level, the pulsing of the second set of cells occurring in groups of one or more cells, each group having a second size smaller than the first size.

6. The method of claim 2, wherein said varying the programming number comprises varying the programming number of the storage cells based upon whether a program pulse comprises an initial pulse or a re-pulse.

7. The method of claim 6, wherein said pulsing the varying programming number of the storage cells comprises:

initially pulsing a set of cells to push the set of cells above a defined threshold, the initial pulsing of the set of cells occurring in groups of two or more cells, each group having a first size larger than that necessary to support predefined variations given the predefined

electrical current provisioning capability of the charge pump;

performing a verification operation on the set of cells; and

if the set of cells fail to verify, re-pulsing the set of cells in groups of one or more cells, each group having a second size smaller than the first size.

8. The method of claim 7, wherein the storage cells comprise multi-level electrically erasable and programmable non-volatile memory cells, the set of cells comprise a first set of cells, and the defined threshold corresponds to a highest level in the multi-level electrically erasable and programmable non-volatile memory cells, and wherein said pulsing the varying programming number of the storage cells further comprises:

pulsing a second set of cells to push those cells toward an intermediate level, the pulsing of the second set of cells occurring in groups of one or more cells, each group having a third size corresponding to the predefined electrical current provisioning capability of the charge pump; and

re-pulsing the second set of cells to push those cells to the intermediate level, the re-pulsing of the second set of cells occurring in groups of two or more cells, each

group having a fourth size larger than the third size.

9. A memory comprising:

an array of electrically erasable and programmable non-volatile memory cells;

a charge pump having an electrical current provisioning capability; and

a variable program bandwidth controller configured to program a varying number of the non-volatile memory cells, which varying number is based upon the electrical current provisioning capability of the charge pump.

10. The memory of claim 9, wherein the non-volatile memory cells comprise flash memory cells.

11. The memory of claim 9, wherein the non-volatile memory cells comprise multi-level electrically erasable and programmable non-volatile memory cells.

12. The memory of claim 11, wherein the varying number is based upon a cell level to be programmed by a pulse.

13. The memory of claim 12, wherein the variable program bandwidth controller pulses a first set of cells in groups of two or more cells to push those cells to an

intermediate level, each group of two or more cells having a first size corresponding to the electrical current provisioning capability, and wherein the variable program bandwidth controller pulses a second set of cells in groups of one or more cells to push those cells to a highest level, each group of one or more cells having a second size smaller than the first size.

14. The memory of claim 9, wherein the varying number is based upon whether a program pulse comprises an initial pulse or a re-pulse.

15. The memory of claim 14, wherein the variable program bandwidth controller pulses a set of cells in groups of two or more cells to push the set of cells above a defined threshold, each group of two or more cells having a first size larger than that necessary to support predefined variations given the electrical current provisioning capability, and wherein the variable program bandwidth controller re-pulses the set of cells in groups of one or more cells if the set of cells fail to verify, each group of one or more cells having a second size smaller than the first size.

16. The memory of claim 15, wherein the non-volatile

memory cells comprise multi-level electrically erasable and programmable non-volatile memory cells, and the defined threshold corresponds to a highest level in the multi-level electrically erasable and programmable non-volatile memory cells.

17. The memory of claim 16, wherein the variable program bandwidth controller comprises a programmable control engine that has been programmed using a control line to enable latching of a command into a microcode program controller.

18. A system comprising:

a processor;

a display coupled with the processor;

an input device coupled with the processor;

an electrically erasable and programmable non-volatile memory coupled with the processor;

a charge pump coupled with the non-volatile memory; and

an execution area configured to program the electrically erasable and programmable non-volatile memory using a variable program bandwidth.

19. The system of claim 18, wherein the variable program bandwidth varies dynamically based upon real-time

program performance and cell current requirements.

20. The system of claim 18, wherein the variable program bandwidth varies based upon a cell level to be programmed by a pulse.

21. The system of claim 18, wherein the variable program bandwidth varies based upon whether a program pulse comprises an initial pulse or a re-pulse.

22. The system of claim 21, wherein the electrically erasable and programmable non-volatile memory comprises a flash memory.

23. The system of claim 22, further comprising a detachable flash memory stick coupled with the processor, the detachable flash memory stick comprising a programmable control engine, the flash memory, the charge pump and the execution area.

24. The system of claim 23, further comprising a transceiver.

25. Microcode for a programmable control engine for a non-volatile memory, the microcode comprising:

instructions to vary a memory programming bandwidth based upon a predefined electrical current provisioning capability; and

instructions to pulse at the varying memory programming bandwidth to store data.

26. The microcode of claim 25, wherein said instructions to vary a memory programming bandwidth comprise instructions to vary the memory programming bandwidth based upon whether a program pulse comprises an initial pulse or a re-pulse.

27. The microcode of claim 26, wherein said instructions to pulse comprise:

instructions to pulse a set of cells to push the set of cells above a defined threshold, the pulsing of the set of cells occurring in groups of two or more cells;

instructions to verify the set of cells; and

failure-condition instructions to re-pulse the set of cells in groups of one or more cells, each group having a second size smaller than the first size.

28. The microcode of claim 26, wherein said instructions to vary a memory programming bandwidth further comprise instructions to vary the memory programming

bandwidth based upon a cell level to be programmed by a pulse.

29. The microcode of claim 28, wherein said instructions to pulse comprise:

instructions to pulse a first set of cells to push those cells to an intermediate level, the pulsing of the first set of cells occurring in groups of three or more cells, each group having a first size;

instructions to pulse a second set of cells to push those cells to a highest level, the pulsing of the second set of cells occurring in groups of two or more cells, each group having a second size smaller than the first size;

instructions to verify cells; and

failure-condition instructions to re-pulse the second set of cells in groups of one or more cells, each group having a third size smaller than the second size.

30. The microcode of claim 29, wherein said instructions to pulse further comprise:

failure-condition instructions to re-pulse the first set of cells to push those cells to the intermediate level, the re-pulsing of the first set of cells occurring in groups of four or more cells, each group having a fourth size larger than the first size.

31. A machine-readable medium embodying information indicative of instructions for causing one or more machines to perform operations comprising:

receiving data to be stored in a non-volatile memory device comprising storage cells and a charge pump having a predefined electrical current provisioning capability;

varying a programming number of the storage cells based upon the predefined electrical current provisioning capability of the charge pump; and

pulsing the varying programming number of the storage cells in the memory device to store the received data in the memory device.

32. The machine-readable medium of claim 31, wherein said varying operation comprises varying the programming number of the storage cells based upon a cell level to be programmed by a pulse.

33. The machine-readable medium of claim 31, wherein said varying operation comprises varying the programming number of the storage cells based upon whether a program pulse comprises an initial pulse or a re-pulse.